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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/729,010 | 12/04/2000 | Michael Ficco | PD-200235 | 6750 |

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Hughes Electronics Corporation
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| EXAMINER | |
|---|---|
| HOFFMAN, BRANDON S | |
| **ART UNIT** | **PAPER NUMBER** |
| 2171 | 2 |

DATE MAILED: 10/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/729,010 | FICCO, MICHAEL | |
| | Examiner | Art Unit | |
| | Brandon Hoffman | 2171 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-53* is/are rejected.

7)☒ Claim(s) *12-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

- Figure 6, reference number 401
- Figure 6, reference number 601
- Figure 6, reference number 407

On page 13 of the specification, with regards to figure 6, the IDE interface 401, FPGA 601, and data path 407 are assigned the wrong numbers. The correct numbers should be IDE interface 301, FPGA 113, and data path 307. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Specification*

2. The disclosure is objected to because of the following informalities:

- On page 2, line 24, "compatible with set-top box" should be –compatible with the set-top box–.
- On page 3, line 13, "well position" should be –well positioned–.
- On page 3, line 22, "comprise" should be –compromise–.
- On page 14, line 14, "interface 13" should be –interface 113–.

Appropriate correction is required.

Claims 12-22 are objected to because of the following informalities:

- Regarding claim 12, "an interface coupled to system bus" should be –an interface coupled to the system bus–.
- Regarding claims 13-22, these claims are dependent on claim 12, and therefore inherit its deficiencies.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-10, 12-20, 23-30, 33-42, 44-51, and 52 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsukamoto et al (U.S. Patent No. 5,796,828).

Regarding claims 1, 33, and 44, Tsukamoto et al. teaches a method/apparatus for storing and retrieving digital data within a hardware platform (figure 2), the method comprising:

- Receiving data bits across a bus of a fixed width, the data bits forming a bit pattern (figure 2, reference numbers 103 and 20);

- Altering the bit pattern of the data bits according to a prescribed scheme (figure 2, reference number 22);
- Storing the altered data bits (figure 2, reference numbers 23A, 24, and 40);
- Restoring the altered data bits to the bit pattern (figure 2, reference number 25); and
- Outputting the restored data bits (figure 2, reference numbers 26 and 105).

Regarding claim 33, specifically, Tsukamoto et al. teaches a computer-readable medium for carrying one or more sequences of one or more instructions for storing and retrieving digital video data within a hardware platform (figure 2, reference number 104A, and column 5, lines 40-52), the one or more sequences of one or more instructions including instructions which, when executed by one or more processors, cause the one or more processors to perform the steps stated in claims 1 and 44, as mentioned above.

Regarding claims 2, 13, 24, 34, and 45, Tsukamoto et al. teaches the altering step comprises inverting a portion of the data bits on the fixed width bus, according to the prescribed scheme (column 4, lines 4-10).

Regarding claims 3, 4, 35, 36, 46 and 47, Tsukamoto et al. teaches wherein the altering step further comprises: scrambling/selectively scrambling the data bits according to the prescribed scheme (column 4, lines 4-10).

Regarding claim 5 and 37, Tsukamoto et al. teaches wherein the altering step and the restoring step are performed by a hard disk drive interface (figure 2, reference number 23A).

Regarding claims 6, 7, 17, 18, 27, 28, 38, 39, 48, and 49, Tsukamoto et al. teaches wherein the prescribed scheme in the step of altering is unique/relatively unique to the hardware platform (figure 2, reference numbers 28A and 29, and column 5, lines 5-10).

Regarding claims 8, 19, 29, 40, and 50, Tsukamoto et al. teaches the prescribed scheme in the step of altering is based upon a serial number of the hardware platform (column 4, lines 12 and 13).

Regarding claims 9, 20, 30, 41 and 51, Tsukamoto et al. teaches (a processor coupled to the system bus for) generating a random number upon power-up of the hardware platform, wherein the prescribed scheme in the step of altering is based upon the random number (figure 2, reference numbers 27, 28A, and 29, and column 4, line 50 to column 5, line 10).

Regarding claims 10, 42, and 52, Tsukamoto et al. teaches wherein the altered bits in the step of altering are stored in a hard disk drive, (the fixed width of the data bits being 16 bits) (column 4, lines 19-28).

Regarding claim 12, Tsukamoto et al. teaches an apparatus for storing and retrieving digital video data (figure 2), comprising:

- A system bus configured to transfer data bits of a fixed width, the data bits forming a bit pattern (figure 2, reference numbers 103, 20 and 21A);
- An interface coupled to system bus and configured to alter the bit pattern of the data bits according to a prescribed scheme (figure 2, reference numbers 22, 23A, and 25); and
- A hard disk drive coupled to the interface and configured to store the altered data bits (figure 2, reference number 40).

Regarding claims 14, 15, 25, and 26, Tsukamoto et al. teaches wherein the interface is further configured to selectively scramble the data bits according to the prescribed scheme (column 4, lines 4-10).

Regarding claims 16, Tsukamoto et al. teaches wherein the apparatus is a digital set-top box (figure 2, reference number 102A).

Regarding claim 23, Tsukamoto et al. teaches a system for storing and retrieving digital audio/video data (figure 2), comprising:

- A satellite antenna configured to receive audio/video signals (figure 2, reference number 103); and

- A set-top box coupled to the satellite antenna (figure 2, reference number 102A), the set-top box comprising,
    - A receiver configured to output data bits corresponding to the received audio/video signals (figure 2, reference number 20),
    - A fixed width bus coupled to the receiver and configured to transfer data bits, the data bits forming a bit pattern (figure 2, reference numbers 20 and 21A),
    - An interface coupled to the bus and configured to alter the bit pattern of the data bits according to a prescribed scheme (figure 2, reference numbers 22, 23A, and 25), and
    - A hard disk drive coupled to the interface and configured to store the altered data bits (figure 2, reference number 40).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 11, 21, 22, 31, 32, 43, and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukamoto et al. (U.S. Patent No. 5,796,828) in view of Goertz (U.S. Patent No. 5,046,065).

Regarding claims 11, 22, 32, 43, and 53, Tsukamoto et al. teaches all of the limitations of claims 1, 12, 23, 33, and 44, respectively. However, Tsukamoto et al. does not teach the bus in the receiving step is a serial bus.

Goertz teaches the bus in the receiving step is a serial bus (column 3, lines 64-68).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to have the bus in the receiving step be a serial bus, as taught by Goertz, to the method of Tsukamoto et al. It would have been obvious to have the bus in the receiving step be a serial bus, as taught by Goertz, to the method of Tsukamoto et al., because a serial bus allows one bit at a time to be processed by a system that can only process one bit a time.

Regarding claims 21 and 31, Tsukamoto et al. teaches all of the limitations of claims 12 and 23, respectively. However, Tsukamoto et al. does not teach the fixed width of the data bits is 16 bits.

Goertz teaches the fixed width of the data bits is 8 bits (column 4, lines 2-5).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine a fixed width of the data bits to be 8 bits, as taught by

Goertz, to the method of Tsukamoto et al. It would have been obvious to combine a fixed width of the data bits to be 8 bits, as taught by Goertz, to the method of Tsukamoto et al., because a fixed width of 8 bits would provide a consistent length of data for the system to manipulate. Although Goertz teaches a fixed width of 8 bits, given the time that the invention was made, a fixed width of 8 bits was the best for that time. A fixed width of 16 bits, or perhaps even 32 bits would be the choice of inventors now because of the increased capacity of the busses and the speed of processors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brandon Hoffman whose telephone number is 703-305-4662. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Safet Metjahic can be reached on 703-308-1436. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Brandon Hoffman

BH
10/15/03

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